REMARKS

Claim 13 is amended to correct a typographical error.

Statutory Double Patenting

Claim 13 is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 19 of prior U.S. Patent No. 6,122,497. Applicant traverses this rejection. Both of these claims read on the embodiment shown in Fig. 15 as noted by the Examiner. However, claim 19 of the prior patent also reads, for example, on the embodiment shown in Fig. 24. Thus, claim 13 of the present application and claim 19 of the prior patent are not coextensive in scope, so the statutory type double patenting rejection is improper.

In the interview summary of the telephonic interview of January 16, 2002, the Examiner notes the possibility of an obviousness type double patenting rejection of claim 13. Any such rejection, however, would be rendered moot by the terminal disclaimer Applicant has submitted to overcome the obviousness type double patenting rejection discussed below.

Obviousness-Type Double Patenting

Claims 2, 3, 9 and 10 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 6,122,497. Applicant submits herewith a terminal disclaimer to obviate this rejection without acquiescing in the propriety of the rejection.

Claim Rejections - 35 USC § 103

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,789,799 to Voinigescu et al. ("Voinigescu") in view of U.S. Patent No. 5,307,512 to Mitzlaff ("Mitzlaff"). Applicant traverses this rejection.

Claim 15 recites first and second class AB input stages arranged to drive the output terminals responsive to first and second input signals, respectively. Support for this claim can be found in the specification at page 20, line 24 through page 21, line11, and in Fig. 26. The Examiner alleges that the first and second class AB input stages recited in claim 15 read on transistors Q1 and Q3, respectively, in Fig. 9 of Voinigescu. However, a class AB stage is understood to have two active devices that deliver power for alternate half cycles. (See generally, pages 378 and 380 of excerpt from Grey & Meyer submitted with the accompanying IDS.) Transistor Q1 in Fig. 9 of Voinigescu could not be a class AB stage because it is a single transistor. Thus, claim 15 is not anticipated by Voinigescu.

Allowable Subject Matter

Claims 16-22 are objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim. These claims have been amended as suggested.

Applicant requests reconsideration in view of the foregoing amendments and remarks. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

13. (Amended twice) A current mirror comprising:

a first transistor having a first terminal and a second terminal coupled together to cause the first transistor to operate as a diode, and a third terminal coupled to a common node;

a first inductor coupled between an input terminal and the first terminal of the first transistor to reduce the noise of the current mirror;

a second transistor having a first terminal for transmitting an output signal, a second terminal coupled to the input terminal, and a third terminal; and

a second inductor coupled between the third terminal of the second transistor and [a] the common node to reduce the noise of the current mirror.

16. (Amended once) An amplifier cell [according to claim 15] comprising:

first and second input terminals;

first and second output terminals;

first class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a first input signal received at the first input terminal; and

a second class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a second input signal received at the second input terminal;

wherein the first class AB input stage comprises:

a first transistor having a first terminal coupled to the first output terminal, a second terminal coupled to receive a bias signal, and a third terminal coupled to receive the first input signal; and

a first current mirror coupled between the first input terminal and the second output terminal.

22. (Amended once) An amplifier cell [according to claim 15] comprising:

first and second input terminals;

first and second output terminals;

first class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a first input signal received at the first input terminal; and

a second class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a second input signal received at the second input terminal;

wherein each of the class AB input stages comprises:

a common base transistor coupled between a first one of the input terminals;

an inductor coupled between the common base transistor and a first one of the output terminals; and

an inductively degenerated current mirror coupled between the first one of the input terminals and the other output terminal.